In the Specification

Please amend the following numbered paragraphs of the specification:

A1

[0029] It should be noted that the present invention applies for any others organizations of the switch matrix such as a 4x4, an 8x8, or a 16x16.

A2

[0032] The FSM logical block 304 performs the following tasks which again are not described in detail herein as they may be executed by common techniques which are not the aim of the invention. The main functions of FSM logical block 304 include receiving packet header detection 224 from selector 302; controlling the memory control circuits 310, 312; sending request_for_connection signals 221 to crossbar data switch 210; receiving grant_connection and acknowledging signals 222 from crossbar data switch 210; controlling the reading of the packets previously stored either into the internal memory or into the expansion memory according to the grant address; and, receiving a general_back_pressure signal 223 from crossbar data switch to inform of an overload of the storing modules to stop sending requests.

A3

[0037] The data_out logical block 205-1 includes a Finite State Machine circuit 402, a Memory control circuit 404 and a Data memory circuit 406. Data memory circuit 406 is connected to the crossbar data switch through the Data_Switch bus 216 to receive data from the select data-in blocks or the expansion data_in blocks. Memory control circuit 404 receives the Data Transfer signal (DATA_XFER) from the crossbar data switch and controls the Write/Read operations of the packets to/from data memory circuit 406. Finite State Machine 402 sends and receives various signals (a General_Back_Pressure signal 223, a Queue_Status signal 225, a Synchronization signal, an External_Back_Pressure signal 226 (EXT_BP)) to control the read operation of a packet to be sent, and to control the overload of the memory.

A4 Cont

[0052] At each synchronization pulse, the switch module ~~analyses~~ analyzes the destination address of each incoming packet (according to the IO's pins configuration as shown in locations 2, 3, and 4 in Table 2) and compares it with its own range address as provided by the address configuration module 220 (Table 1). If the destination address falls within the range of the module,

then the packet is output within a data-out block 204 of this latter, otherwise the packet is rerouted on the respective expansion data-out circuit 208 based on the packet bits configuration.

[0053] In the case where the bits configuration of the incoming packet is in the range of the corresponding module, then the select data-in circuit 203-1 to 203-8 receiving this incoming packet sends the packet to its internal memory 306 through the internal bus 316 as previously described with FIG. 3 and validates the incoming packet by setting the valid_packet signal 318.

[0054] Referring to FIG. 8A, consider as an example where the configuration is a 3-modules card connected together such as to be in the ports expansion mode and interconnecting 24 LAN's adapters. If the LAN adapter connected to port denoted 'S1' of first module 800 wants to send a frame to the LAN adapter connected to port 'Out-16' of second module 802, the LAN adapter splits the frame in '53 + 1 = 54' bytes packets wherein the header contains the final destination address ('Out-16' in the present example). The destination address byte of the packet incoming to port 'S1' of the first module is analyzed by the select data-in function and based on the configuration module reroutes the packet without the need of changing the destination switch module. In the present example the packet is rerouted to first expansion data-out block 209-1 of first module, and then ~~send~~ sent to the first expansion data-in block 207-1 of second module where it is stored in the expansion memory 506 in order to be later processed by the crossbar mechanism of the crossbar data switch 210 of second module to be switched to the appropriated output. As soon as the packet is stored into the expansion memory of second module, the expansion mechanism sends a request for connection signal to the crossbar data switch in order to request a connection to port 'Out-16'. The crossbar sends back an acknowledge signal in order to inform that the connection will be established at the synchronization pulse. At the next synchronization pulse, the expansion-in function puts the appropriate data onto the expansion-mux-bus 214-1 and the packet is transferred through the crossbar data switch to the destination data-out block 205-8 to be sent finally to the connected LAN adapter.